Edit an existing query or compose a new query in the Search Query Display.

Select a search number (#) to:

- Add a query to the Search Query Display
- Combine search queries using AND, OR, or NOT
- Delete a search
- Run a search

Mon, 25 Jul 2005, 6:53:26 AM EST

Search Query Display

Recent Search Queries

#1 ((kimura and semiconductor and analyzer)<in>metadata)

#2 ((semiconductor and analyzer)<in>metadata)

#3 (semiconductor and analyzer and y-matrix<IN>metadata)

#4 (semiconductor and analyzer and y-matrix<IN>metadata)

Results for "**(semiconductor and analyzer and y-matrix<in>metadata)**" e-mail
Your search matched **2** of **1194402** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» Search Options

View Session History

New Search

Modify Search

(semiconductor and analyzer and y-matrix<in>metadata)

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information

1. **Element extraction of GaAs dual-gate MESFET small-signal equivalent ci**
Wei-Kung Deng; Tah-Hsiung Chu;
Microwave Theory and Techniques, IEEE Transactions on
Volume 46, Issue 12, Part 2, Dec. 1998 Page(s):2383 - 2390
Digital Object Identifier 10.1109/22.739226
AbstractPlus | References | Full Text: PDF(304 KB) IEEE JNL

2. **Identification of MOS oxide defect location with a spatial resolution less t using photoemission microscope**
Ohzone, T.; Yuzaki, M.; Matsuda, T.; Kameda, E.;
Microelectronic Test Structures, 1999. ICMTS 1999. Proceedings of the 1999 I Conference on
15-18 March 1999 Page(s):89 - 94
Digital Object Identifier 10.1109/ICMTS.1999.766222
AbstractPlus | Full Text: PDF(516 KB) IEEE CNF

Dialog DataStar

options | logoff | feedback | help

databases | easy search

Advanced Search: INSPEC - 1969 to date (INZZ)

limit

Search history:

No.	Database	Search term	Info added since	Results	
1	INZZ	semiconductor AND analyzer AND y-matrix	unrestricted	0	-

hide | delete all search steps... | delete individual search steps...

Enter your search term(s): Search tips

whole document

Information added since: or: none
(YYYYMMDD)

search

Select special search terms from the following list(s):

- Publication year
- Classification codes A: Physics, 0-1
- Classification codes A: Physics, 2-3
- Classification codes A: Physics, 4-5
- Classification codes A: Physics, 6
- Classification codes A: Physics, 7
- Classification codes A: Physics, 8
- Classification codes A: Physics, 9
- Classification codes B: Electrical & Electronics, 0-5
- Classification codes B: Electrical & Electronics, 6-9
- Classification codes C: Computer & Control
- Classification codes D: Information Technology
- Classification codes E: Manufacturing & Production
- Treatment codes
- INSPEC sub-file
- Language of publication

Terms used **semiconductor** and **analyzer** and **y matrix** Found **394** of **158,639**

Sort results by relevance

Display results expanded form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Best 200 shown Relevance scale

1 Determination of worst-case aggressor alignment for delay calculation

Paul D. Gross, Ravishankar Arunachalam, Karthik Rajagopal, Lawrence T. Pileggi

November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(883.15 KB) Additional Information: full citation, references, citings, index terms

2 RAP. 2 - an Associative Processor for data bases

S. A. Schuster, H. B. Nguyen, E. A. Ozkarahan, K. C. Smith

April 1978 **Proceedings of the 5th annual symposium on Computer architecture**

Full text available: pdf(815.27 KB) Additional Information: full citation, abstract, references, citings, index terms

RAP - a Relational Associative Processor - is a back-end or peripheral device to augment a general purpose computer for implementing a data base management system (DBMS). Its architecture is based on the fact that data base operations are inherently set-oriented and that data base addressing is best accomplished through associative reference to achieve high data independence. RAP utilizes these characteristics by combining the features of associative and array processors. Previous publicati ...

3 Capacity planning for semiconductor wafer fabrication with time constraints between operations

Jennifer K. Robinson, Richard Giglio

December 1999 **Proceedings of the 31st conference on Winter simulation: Simulation---a bridge to the future - Volume 1**

Full text available: pdf(93.05 KB) Additional Information: full citation, references, citings, index terms

4 The augmented predictive analyzer for context-free languages—its relative efficiency

Susumu Kuno

November 1966 **Communications of the ACM**, Volume 9 Issue 11

Full text available: pdf(1.63 MB) Additional Information: full citation, abstract, references, citings

It has been proven by Greibach that for a given context-free grammar G, a standard-form grammar Gs, can be constructed, which generates the same language as is generated by G and whose rules are all of the form $Z \rightarrow cY1 \cdots Ym$ $(m \geqslant 0)$ where Z and Yi are

intermediat ...

5 Evaluation of lot release policies for semiconductor manufacturing systems
Raka Sandell, Krishna Srinivasan
November 1996 **Proceedings of the 28th conference on Winter simulation**
Full text available: pdf(948.03 KB) Additional Information: full citation, references

6 Semiconductor manufacturing: Scheduling and dispatching: scheduling batch processing machines in complex job shops
Kasin Oey, Scott J. Mason
December 2001 **Proceedings of the 33nd conference on Winter simulation**
Full text available: pdf(257.86 KB) Additional Information: full citation, abstract, references, index terms

This paper considers a complex job shop problem with reentrant flow and batch processing machines. A modified shifting bottleneck heuristic (MSB) is considered for generating machine schedules to minimize the total weighted tardiness. We observe that the MSB could produce infeasible schedules where cyclic schedules are found. A cycle elimination procedure is proposed to remove the possibility of the MSB generating cyclic schedules in the solution.

7 Session 9D: new approaches to at-speed BIST and diagnosis: Error catch and analysis for semiconductor memories using march tests
Chi Feng Wu, Chih Tsun Huang, Chih Wea Wang, Kuo Liang Cheng, Cheng Wen Wu
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(85.96 KB) Additional Information: full citation, abstract, references, citings

We present an *error catch and analysis* (ECA) system for semiconductor memories. The system consists of a test algorithm generator called TAGS, a fault simulator called RAMSES, and an error analyzer (ERA). We use TAGS to generate a set of test algorithms of different lengths and diagnostic resolutions for the memory under test, and use RAMSES to generate the *March dictionary* for each test algorithm. With the March dictionaries, ERA is able to support March algorithms for easy diagn ...

8 Analysis of FPGA/FPIC switch modules
Yao-Wen Chang, Kai Zhu, Guang-Ming Wu, D. F. Wong, C. K. Wong
January 2003 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 8 Issue 1
Full text available: pdf(508.09 KB) Additional Information: full citation, abstract, references, index terms, review

Switch modules are the most important component of the routing resources in FPGAs/FPICs. Previous works have shown that switch modules with higher routability result in better area performance for practical applications. We consider in this paper an FPGA/FPIC switch-module analysis problem: the inputs consist of a switch-module description and the number of nets required to be routed through the switch module; the question is to determine if there exists a feasible routing for the routing requir ...

Keywords: Computer-aided design of VLSI, FPGA, FPIC, layout, synthesis

9 Performance prediction tools for parallel discrete-event simulation
Chu-Cheow Lim, Yoke-Hean Low, Boon-Ping Gan, Sanjay Jain, Wentong Cai, Wen Jing Hsu, Shell Ying Huang

May 1999 **Proceedings of the thirteenth workshop on Parallel and distributed simulation**

Full text available: pdf(788.70 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We have developed a set of performance prediction tools which help to estimate the achievable speedups from parallelizing a sequential simulation. The tools focus on two important factors in the actual speedup of a parallel simulation program : (a) the simulation protocol used, and (b) the inherent parallelism in the simulation model. The first two tools are a performance/parallelism analyzer for a conservative, asynchronous simulation protocol, and a similar analyzer for a conservative, synchro ...

10 Repeater insertion method and its application to a 300MHz 128-bit 2-way superscalar microprocessor

Norman Kojima, Yukiko Parameswar, Christian Klingner, Yukio Ohtaguro, Masataka Matsui, Shigeaki Iwasa, Tatsuo Teruyama, Takayoshi Shimazawa, Hideki Takeda, Kouji Hashizume, Haruyuki Tago, Masaaki Yamada

January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Full text available: pdf(288.26 KB) Additional Information: full citation, references, citings

11 Extending high performance Fortran for the support of unstructured computations

Andreas Müller, Roland Rühl

July 1995 **Proceedings of the 9th international conference on Supercomputing**

Full text available: pdf(1.33 MB) Additional Information: full citation, references, citings, index terms

12 An application of simulation to tracking

David A. Bennett, Christopher A. Landauer

December 1979 **Proceedings of the 11th conference on Winter simulation - Volume 1**

Full text available: pdf(720.76 KB) Additional Information: full citation, abstract, references, index terms

The AIMER project (Automatic Integration of Multiple Element Radars) is an emulated model of a loosely coupled distributed radar tracking processor. The computational elements of the model are minicomputers similar to the PDP-11. Design goals of the model are to provide a reliable processing system whose computational bandwidth can be dynamically altered in response to changing ground scenario and availability of hardware. A large number of minicomputers connected with multiple packet netwo ...

Keywords: Active radar tracking, Distributed processing, Microprogramming, Network operating system, Performance monitoring, Simulation/emulation

13 Novel DFT, BIST and diagnosis techniques: Effective diagnostics through interval unloads in a BIST environment

Peter Wohl, John A. Waicukauski, Sanjay Patel, Greg Maston

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(155.82 KB) Additional Information: full citation, abstract, references, citings, index terms

Logic built-in self test (BIST) is increasingly being adopted to improve test quality and reduce test costs for rapidly growing designs. Compared to deterministic automated test pattern generation (ATPG), BIST presents inherent fault diagnostic challenges. Previous

diagnostic techniques have been limited in their diagnosis resolution and/or require significant hardware overhead. This paper proposes an interval-based scan-unload method that ensures diagnosis resolution down to gate-level faults ...

Keywords: built-in self-test (BIST), fault diagnosis

14 Managing battery lifetime with energy-aware adaptation

Jason Flinn, M. Satyanarayanan

May 2004 **ACM Transactions on Computer Systems (TOCS)**, Volume 22 Issue 2

Full text available: pdf(1.61 MB) Additional Information: full citation, abstract, references, index terms

We demonstrate that a collaborative relationship between the operating system and applications can be used to meet user-specified goals for battery duration. We first describe a novel profiling-based approach for accurately measuring application and system energy consumption. We then show how applications can dynamically modify their behavior to conserve energy. We extend the Linux operating system to yield battery lifetimes of user-specified duration. By monitoring energy supply and demand and ...

Keywords: Power management, adaptation

15 WTA: waveform-based timing analysis for deep submicron circuits

Larry McMurchie, Carl Sechen

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(219.96 KB) Additional Information: full citation, abstract, references, citings, index terms

Existing static timing analyzers make several assumptions about circuits, implicitly trading off accuracy for speed. In this paper we examine the validity of these assumptions, notably the slope approximation to waveforms, single-input transitions, and the choice of a propagating signal based on a single voltage-time point. We provide data on static CMOS gates that show delays obtained in this way can be optimistic by more than 30%. We propose a new approach, Waveform-based Timing Analysis that ...

16 Symmetric transparent BIST for RAMs

S. Hellebrand, H.-J. Wunderlich, V. N. Yarmolik

January 1999 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(53.25 KB) Additional Information: full citation, index terms

17 Design innovations for embedded processors: A fast on-chip profiler memory

Roman Lysecky, Susan Cotterell, Frank Vahid

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(277.15 KB) Additional Information: full citation, abstract, references, citings, index terms

Profiling an application executing on a microprocessor is part of the solution to numerous software and hardware optimization and design automation problems. Most current profiling techniques suffer from runtime overhead, inaccuracy, or slowness, and the traditional non-intrusive method of using a logic analyzer doesn't work for today's system-on-a-chip having embedded cores. We introduce a novel on-chip memory architecture that overcomes these limitations. The architecture, which we call ProMem ...

Keywords: adaptive architectures, binary tree, embedded CAD, embedded systems, low

power, memory design, platform tuning, profiling, system-on-a-chip

18 Simulation of a distributed system for performance modelling
David A. Bennett, Christopher A. Landauer
August 1979 **Proceedings of the 1979 ACM SIGMETRICS conference on Simulation, measurement and modeling of computer systems**, Volume 8 , 11 Issue 3 , 1
Full text available: pdf(682.40 KB) Additional Information: full citation, abstract, references, index terms

A distributed system of cooperating minicomputers is simulated by AIMER (Automatic Integration of Multiple Element Radars) to model and analyze the behavior of a radar tracking system. Simulation is applied in the AIMER project in an attempt to model a network of minicomputers to discover a maximally flexible network architecture. Because building the tracking system out of real hardware would not result in a flexible enough testbed system, the proposed configuration is represented by a sof ...

19 Designing SoCs for yield improvement: Embedding infrastructure IP for SOC yield improvement
Yervant Zorian
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(220.88 KB) Additional Information: full citation, abstract, references, citings, index terms

In addition to the functional IP cores, today's SOC necessitates embedding a special family of IP blocks, called Infrastructure IP blocks. These are meant to ensure the manufacturability of the SOC and to achieve adequate levels of yield and reliability. The Infrastructure IP leverages the manufacturing knowledge and feeds back the information into the design phase. This paper analyzes the key trends and challenges resulting in manufacturing susceptibility and field reliability that necessitate ...

Keywords: embedded test & repair, semiconductor IP, test resource partitioning, yield optimization

20 Testing: Hierarchical extreme-voltage stress test of analog CMOS ICs for gate-oxide reliability enhancement
Chin-Long Wey, M. A. Khalil, Jim Liu, Gregory Wierzba
April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**
Full text available: pdf(224.23 KB) Additional Information: full citation, abstract, references, index terms

Yield and reliability are two factors affecting the profitability of semiconductor manufacturing. High-temperature burn-in and extreme-voltage stress tests are two current industrial standard methods to speed up the deterioration of electronic devices and weed-out infant mortality. Extreme-voltage stress test aims at enhancing both quality and reliability without performance the high-cost burn-in test process. Our recent stress tests of analog/mixed-signal CMOS ICs for gate-oxide reliability enh ...

Keywords: IC reliability

results **1 - 6**

6 Articles Found

pub-date > 1994 and semiconductor and analyzer and y-matrix

1. **FEM based damping studies of metastable Al/Ti composites** • ARTICLE
Journal of Alloys and Compounds, Volume 394, Issues 1-2, 17 May 2005, Pages 226-234
Narasimalu Srikanth and Manoj Gupta
SummaryPlus | Full Text + Links | PDF (411 K)

2. **On-line multi-analyzer monitoring of biomass, glucose and acetate for growth rate control of a *Vibrio cholerae* fed-batch cultivation** • ARTICLE
Journal of Biotechnology, Volume 115, Issue 1, 12 January 2005, Pages 67-79
Marián Navrátil, Anna Norberg, Lars Lembrén and Carl-Fredrik Mandenius
SummaryPlus | Full Text + Links | PDF (392 K)

3. **MEMS-based series and shunt variable capacitors for microwave and millimeter-wave frequencies** • ARTICLE
Sensors and Actuators A: Physical, Volume 91, Issue 3, 15 July 2001, Pages 256-265
Zhiping Feng, Huantong Zhang, K. C. Gupta, Wenge Zhang, Victor M. Bright and Y. C. Lee
SummaryPlus | Full Text + Links | PDF (791 K)

4. **Computationally efficient large-change statistical analysis of linear electronic circuits** • ARTICLE
Microelectronics Reliability, Volume 40, Issue 6, 1 June 2000, Pages 1023-1038
T. Ili¿, V. B. Litovski, I. V. Litovski and S. Stojiljkovi¿
Abstract

5. **Analysis of breath alcohol with a multisensor array: instrumental setup, characterization and evaluation** • ARTICLE
Forensic Science International, Volume 105, Issue 2, 1 November 1999, Pages 95-114
Nils J. P. Paulsson and Fredrik Winquist
SummaryPlus | Full Text + Links | PDF (446 K)

6. **Effect of thermal history on creep behaviour of a Cu-16Al solid solution alloy** • ARTICLE
Scripta Metallurgica et Materialia, Volume 33, Issue 6, 15 September 1995,

Pages 1013-1019
M. Pahutová, V. Šustek and J. Čadek
Abstract

6 Articles Found

pub-date > 1994 and semiconductor and analyzer and y-matrix

Edit Search | Save Search | Save as Search Alert

results **1 - 6**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	("kimura.in. andsemiconductorandanalyzer"). PN.	USPAT; USOCR	OR	OFF	2005/07/25 07:01
L2	0	("semiconductorandanalyzerandy-matrix").PN.	USPAT; USOCR	OR	OFF	2005/07/25 07:01